UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/732,763	12/10/2003	Masaru Doi	02008.135001	6966

22511 7590 09/06/2006

OSHA LIANG L.L.P.
1221 MCKINNEY STREET
SUITE 2800
HOUSTON, TX 77010

EXAMINER	
SIEVERS, LISA C	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/732,763	DOI ET AL.	
	Examiner	Art Unit	
	Lisa C. Sievers	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-15,17,18 and 20-29* is/are rejected.

7)☒ Claim(s) *8,16 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08142006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

2. Should applicant desire to obtain the benefit of a continuation of PCT/JP02/05924, a certified translation of the Japanese document should be submitted in reply to this action.

3. Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d), a certified translation of the foreign application should be submitted in reply to this action.

Drawings

4. Figures 25 - 29 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

5. The information disclosure statements filed on 2/10/2003 and 8/14/2006 fail to comply with 37 CFR 1.98(a)(3) because they do not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Specification

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 8, 16 and 19 are objected to because of the following informalities:

7. Claims 8, 16 and 19 depend on rejected claims and include all the limitations thereof, therefore, these dependent claims are objected to.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 26 - 29 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 26 - 29 do not produce any tangible results. The practical application of the claimed invention cannot be realized until the information determined is conveyed to the user. For the result to be tangible, it would need to be output to a user or displayed to a user or stored for later use. For further guidance, applicant is referred to the November, 2005 O.G. Notice available at the PTO internet site:
http://www.uspto.gov/web/offices/com/sol/og/2005/week47/patgupa.htm.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

9. Claims 1 – 7, 13 – 15, 17 – 18, 20 – 22, 26 and 28 are rejected under 35 U.S.C. 102(a) as being anticipated by Miura (JP 2001-201532).

With respect to claim 1, Miura (JP 2001-201532) teaches an apparatus for testing a semiconductor device (Miura (JP 2001-201532), claim 1) based on output data of said semiconductor device, comprising: a multi-strobe generator [30, 34] for generating a multi-strobe having a plurality of strobes, of which phases are different by a small amount (Miura (JP 2001-201532), figures 3 – 4; claim 2, line 3); an output data transition point detector [11] for detecting a timing of rising or falling of a waveform of said output data based on said multi-strobe (Miura (JP 2001-201532), drawing 1; [0004], lines 6 – 8; [0008]; [0041]); a

reference clock transition point detector [10, TC1 - TCn] for detecting a timing of rising or falling of a reference clock [DQS] outputted by said semiconductor device accompanying said output data, wherein said reference clock [DQS] is a signal to set a timing of passing said output data, based on said multi-strobe (Miura (JP 2001-201532), drawing 1; [0002], lines 7 – 9); and a judging unit [12 and PF1 – PFn] for judging quality of said semiconductor device based on said timing of rising or falling of a waveform of said output data detected by said output data transition point detector [11] and said timing of rising or falling of a waveform of said reference clock [DQS] detected by said reference clock transition point detector [10, TC1 – TCn]. (Miura (JP 2001-201532), drawing 1; [0007] – [0009])

With respect to claim 2, Miura (JP 2001-201532) additionally teaches wherein said judging unit [12 and PF1 – PFn, respectfully] judges quality of said semiconductor device based on whether or not a phase difference between said timing of rising or falling of a waveform of said output data detected by said output data transition point detector [11] and said timing of rising or falling of a wave form of said reference clock [DQS] detected by said reference clock transition point detector [10, TC1 – TCn] is within a predetermined range. (Miura (JP 2001-201532), drawing 10, [0003])

With respect to claim 3, Miura (JP 2001-201532) additionally teaches wherein said multi-strobe generator [34] generates a first multi-strobe in order to detect a transition point of a value of said output data and a second multi-strobe in order to detect a transition point of a value of said reference clock [DQS]. (Miura (JP 2001-201532), drawing 1)

With respect to claim 4, Miura (JP 2001-201532) additionally teaches the apparatus further comprising a level comparator [12, PF1 - PFn] for changing said output data and said reference clock [DQS] into digital data represented by H logic or L logic (Miura (JP 2001-201532), [0007] – [0010]), wherein said output data transition point detector [11] detects a value of said output data changed into said digital data in regard to a phase of each of strobes of said first multi-

strobe (Miura (JP 2001-201532), drawing 1, [0008] – [0009]), and if a value of said output data in regard to a phase of a first strobe of said first multi-strobe and a value of said output data in regard to a phase of a second strobe adjacent to said first strobe are different then determines said phase of said first strobe as said transition point of said value of said output data (Miura (JP 2001-201532), [0009] – [0010]), said reference clock transition point detector [10, TC1 – TCn] detects a value of said reference clock [DQS] changed into said digital data in regard to a phase of each of strobes of said second multi-strobe, and if a value of said reference clock [DQS] in regard to a phase of a third strobe of said second multi-strobe and a value of said reference clock [DQS] in regard to a phase of a fourth strobe adjacent to said third strobe are different then determines said phase of said third strobe as said transition point of said value of said reference clock [DQS] (Miura (JP 2001-201532), drawings 3 – 4), and said judging unit [12, PF1 – PFn] judges quality of said semiconductor device based on said transition point of said value of said output data and said transition point of said value of said reference clock [DQS] (Miura (JP 2001-201532), drawing 10, [0003]).

With respect to claim 5, Miura (JP 2001-201532) additionally teaches wherein said judging unit [12, PF1 – PFn] judges quality of said semiconductor device based on whether or not a difference between a strobe number of said first multi-strobe indicating which timing of a strobe of said first multi-strobe said output data transition point detector [11] detects said transition point of a value of said output data and a strobe number of said second multi-strobe indicating which timing of a strobe of said second multi-strobe said reference clock transition point detector [10, TC1 – TCn] detects said transition point of a value of said reference clock [DQS] at is within a predetermined range. (Miura (JP 2001-201532), [0018], claim 3)

With respect to claim 6, Miura (JP 2001-201532) additionally teaches wherein said judging unit [12, PF1 – PFn, 31, 32] comprises a memory for storing a reference table [drawing 6] to set quality of said semiconductor device about a combination of said strobe number of said first multi-strobe, in which said

transition point of a value of said output data is detected and said strobe number of said second multi-strobe, in which said transition point of a value of said reference clock [DQS] is detected, and judges quality of said semiconductor device based on said reference table. (Miura (JP 2001-201532), drawing 6, [0036])

With respect to claim 7, Miura (JP 2001-201532) additionally teaches wherein said output data transition point detector [11] comprises a means for detecting whether a value of digital data in regard to said transition point of a value of said output data changes from said H logic to said L logic or changes from said L logic to said H logic. (Miura (JP 2001-201532), [0009])

With respect to claim 13, Miura (JP 2001-201532) additionally teaches wherein said multi-strobe generator [30] comprises a plurality of delay devices [DY1 – DYn] having different delay times, supplies a strobe to each of said plurality of delay devices and outputs a plurality of strobes, delayed to have a different time delay respectively and outputted by said plurality of delay devices [DY1 – DYn], as said multi-strobe. (Miura (JP 2001-201532), drawing 1, [0027], [0045])

With respect to claim 14, Miura (JP 2001-201532) additionally teaches wherein said multi-strobe generator [30] comprises a plurality of delay devices [DY1 – DYn] connected in cascade (Miura (JP 2001-201532), [0045], lines 2 –3), supplies a strobe to each of said plurality of delay devices [DY1 – DYn] connected in cascade and generates said multi-strobe based on strobes delayed respectively and outputted by said plurality of delay devices. (Miura (JP 2001-201532), drawing 1)

With respect to claim 15, Miura (JP 2001-201532) teaches an apparatus for testing a semiconductor device (Miura (JP 2001-201532), claim 1) based on output data of said semiconductor device, comprising: a first multi-strobe generator [30, 34] for generating a first multi-strobe having a plurality of strobes, of which phases are different by a small amount in regard to said output data (Miura (JP 2001-201532), claim 2, line 3; [0041]); a reference phase measuring

unit [31] for measuring an output timing (Miura (JP 2001-201532), [0036]), which is a signal to set a timing of passing said output data, being a timing of rising or falling of a waveform of a reference clock [DQS] outputted by said semiconductor device accompanying said output data (Miura (JP 2001-201532), drawing 1; [0002], lines 7 – 9); a reference phase memory [32] for memorizing said output timing (Miura (JP 2001-201532), [0036], line 14); a transition point detector [11] for detecting a transition point of a value of said output data based on said first multi-strobe (Miura (JP 2001-201532), drawing 1; [0004], lines 6 – 8; [0008]; [0041]); a phase difference measuring unit [30, 31, 32, 33, 34] for measuring a phase difference between said output timing and said transition point of a value of said output data (Miura (JP 2001-201532), drawing 1, [0040]); and a judging unit [12] for judging quality of said semiconductor device based on said phase difference. (Miura (JP 2001-201532), drawing 10, [0003])

With respect to claim 17, Miura (JP 2001-201532) additionally teaches wherein said transition point detector [11] comprises a means [12] for changing said output data into digital data represented by H logic or L logic (Miura (JP 2001-201532), [0009]), and said transition point detector [11] detects a value of said output data in regard to a phase of each of strobes [P1 – P5] of said first multi-strobe, and if a value of digital data in regard to a phase of a first strobe [P1] of said first multi-strobe and a value of digital data in regard to a phase of a second strobe [P2] adjacent to said first strobe are different then determines said phase of said first strobe as said transition point of said value of said output data. (Miura (JP 2001-201532), drawings 3 and 4)

With respect to claim 18, Miura (JP 2001-201532) additionally teaches wherein said transition point detector [11] comprises a means for detecting whether said value of digital data in regard to said transition point changes from said H logic to said L logic or changes from said L logic to said H logic. (Miura (JP 2001-201532), [0008] – [0010])

With respect to claim 20, Miura (JP 2001-201532) additionally teaches wherein said reference phase measuring unit [30, 31, 32, 33, 34] comprises: a

means [30] for generating a second multi-strobe having a plurality of strobes, of which phases are different by a small amount (Miura (JP 2001-201532), claim 2, line 3), in regard to said reference clock [DQS]; a means [10, TC1 – TCn] for detecting said transition point of a value of said reference clock [DQS] based on said second multi-strobe; and a means for calculating said output timing of said reference clock [DQS] based on a strobe number of said second multi-strobe, in which said transition point of a value of said reference clock [DQS] is detected (Miura (JP 2001-201532), drawing 13, [0040]).

With respect to claim 21, Miura (JP 2001-201532) additionally teaches wherein said reference phase memory [32] stores said strobe number of said second multi-strobe, in which said transition point of a value of said reference clock [DQS] is detected. (Miura (JP 2001-201532), [0044], lines 5 – 10)

With respect to claim 22, Miura (JP 2001-201532) additionally teaches an wherein said first multi-strobe generator [34] sets a phase of said first multi-strobe based on said strobe number of said second multi-strobe stored by said reference phase memory [32]. (Miura (JP 2001-201532), [0040]; [0044], lines 10 - 13)

With respect to claim 26, Miura (JP 2001-201532) teaches a method for testing a semiconductor device (Miura (JP 2001-201532), claim 1) based on output data of said semiconductor device, comprising: a first multi-strobe generating step of generating a first multi-strobe having a plurality of strobes, of which phases are different by a small amount in regard to said output data (Miura (JP 2001-201532), claim 2, line 3; [0041]); an output data transition point detecting step of detecting a timing of rising or falling of a waveform of said output data based on said first multi-strobe (Miura (JP 2001-201532), drawing 1; [0004], lines 6 – 8; [0008]; [0041]); a second multi-strobe generating step of generating a second multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to a reference clock [DQS] (Miura (JP 2001-201532), claim 2, line 3), which is a signal to set a timing of passing said output data, said reference clock [DQS] being outputted by said semiconductor

device accompanying said output data (Miura (JP 2001-201532), drawing 1; [0002], lines 7 – 9); a reference clock transition point detecting step of detecting a timing of rising or falling of a waveform of said reference clock [DQS] based on said second multi-strobe (Miura (JP 2001-201532), drawing 1; [0007] – [0009]); and a judging step of judging quality of said semiconductor device based on said timing of rising or falling of a waveform of said output data detected in said output data transition point detecting step and said timing of rising or falling of a waveform of said reference clock [DQS] detected in said reference clock transition point detecting step. (Miura (JP 2001-201532), drawing 1; [0007] – [0009])

With respect to claim 28, Miura (JP 2001-201532) teaches a method for testing a semiconductor device (Miura (JP 2001-201532), claim 1) based on output data of said semiconductor device, comprising: a reference phase measurement step of measuring an output timing of a reference clock [DQS] (Miura (JP 2001-201532), [0036]), which is a signal to set a timing of passing said output data, said reference clock [DQS] being outputted by said semiconductor device accompanying said output data (Miura (JP 2001-201532), drawing 1; [0002], lines 7 – 9); a reference phase memorizing step of memorizing said output timing (Miura (JP 2001-201532), [0036], line 14); a first multi-strobe generating step of generating a first multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to said output data (Miura (JP 2001-201532), claim 2, line 3; [0041]); an output data transition point detecting step of detecting said transition point of a value of said output data based on said first multi-strobe (Miura (JP 2001-201532), drawing 1; [0004], lines 6 – 8; [0008]; [0041]); a phase difference measuring step of measuring a phase difference between said output timing and said transition point of a value of said output data (Miura (JP 2001-201532), [0040]); and a judging step of judging quality of said semiconductor device based on said phase difference. (Miura (JP 2001-201532), drawing 10, [0003])

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 9 – 12, 23 – 25, 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura (JP 2001-201532) in view of Shimonaka (JP 2000-162290).

With respect to claims 9 – 12, Miura (JP 2001-201532) teaches the invention, as set forth above under the rejection of claim 1.

With respect to claims 23 – 25, Miura (JP 2001-201532) teaches the invention, as set forth above under the rejection of claim 15.

With respect to claim 27, Miura (JP 2001-201532) teaches the invention, as set forth above under the rejection of claim 26.

With respect to claim 29, Miura (JP 2001-201532) teaches the invention, as set forth above under the rejection of claim 28.

With respect to claims 9, 11 and 23, Miura (JP 2001-201532) does not teach a semiconductor testing device further comprising a glitch detector for detecting existence of a glitch in regard to said output data based on said timing of rising or falling of a waveform of said output data detected by said output data transition point detector (claim 9) or based on the transition point of a value of said output data (claims 11 and 23).

With respect to claims 10 and 24, Miura (JP 2001-201532) does not teach wherein the judging unit judges quality of said semiconductor device further based on existence of a glitch detected by a glitch detector.

With respect to claims 12 and 25, Miura (JP 2001-201532) does not teach wherein a glitch detector judges that there is a glitch of said output data if the transition points of a value of said output data are more than or equal to two.

With respect to claim 27, Miura (JP 2001-201532) does not teach a method further comprising a glitch detecting step of detecting existence of a glitch in regard to said output data based on said transition point of a value of said output data, wherein said judging step judges quality of said semiconductor device further based on existence of said glitch detected in said glitch detecting step.

With respect to claim 29, Miura (JP 2001-201532) does not teach a method further comprising a glitch detecting step of detecting existence of a glitch in regard to said output data based on said transition point of a value of said output data.

Shimonaka (JP 2000-162290) teaches a glitch detector and glitch detecting step for a semiconductor tester that examines a first signal and then a second signal, monitoring for changes in the logical level of the initial stimulus. For a low level stimulus, a glitch is detected when the level of a stimulus becomes more than or equal to two. (Shimonaka (JP 2000-162290), [0009], [0024])

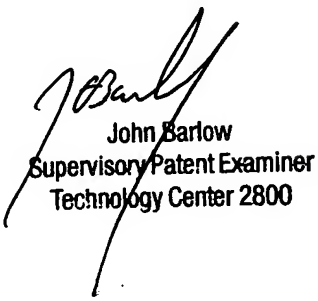
It would have been obvious to one of ordinary skill in the art, at the time the invention was made for Miura (JP 2001-201532) to have included the glitch detector, with its stimulus thresholds at two and above (claims 12 and 25), of Shimonaka (JP 2000-162290) in the analysis of the rising and falling of waveforms (claim 9) and transition points of the output data (claims 10, 11, 23, 24, 27 and 29) because it provides a quick, easy, and reliable method to address potential problems in semiconductor testing. (Shimonaka (JP 2000-162290), Patent Abstract, [0029])

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lisa C. Sievers whose telephone number is (571) 272-8052. The examiner can normally be reached on M-F, 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



LCS

Lisa.Sievers@USPTO.gov